800G OSFP SR8 Transceiver

S-OS800G31M1601-CD

Product Features

- 8 independent parallel optical channels
- Each channel data rate up to 53.12GBaud with CDR
- Hot Pluggable
- Up to 100m link over OM4 Multi-mode
- 850nm VCSEL/PD Array Technology
- OSFP MSA Compliance
- MPO-16 APC Optical Receptacle Type
- Monitors for VCSEL bias,transmitted,received power,module temperature,and module supply
- Case Operating Temperature Range: Commercial: 0 to 70ºC
- RoHS II Compliance
- CMIS5.0 Compliance

Product Applications

- High performance computing interconnect
- Data center

General

The S-OS800G31M1601-CD is a OSFP Optical transceiver for 8 x 53.12GBaud optical links. It is compliant with the OSFP MSA specifications. It operates at 53.12GBaud up to 100m over OM4 Multi-mode fiber.

Performance Specifications

Absolute Maximum Ratings					
Parameter	**Symbol**	**Min.**	**Max.**	**Unit**	**Note**
Storage Temperature	T_{stg}	-40	+85	℃	
Relative Humidity - Storage	R_{HS}	0	95	%	
Relative Humidity - Operating	R_{HO}	0	85	%	
Supply Voltage	V_{CC}	-0.5	+3.6	V	

Recommended Operating Conditions						
Parameter	**Symbol**	**Min.**	**Typical**	**Max.**	**Unit**	**Note**
Operating Case Temperature	T_C	0	25	+70	℃	
Power Supply Voltage	V_{CC}	3.14	3.30	3.46	V	
Power Consumption	P	-	13.2	-	W	
Signaling Speed Per Channel	S	-	53.12	-	Gbaud	

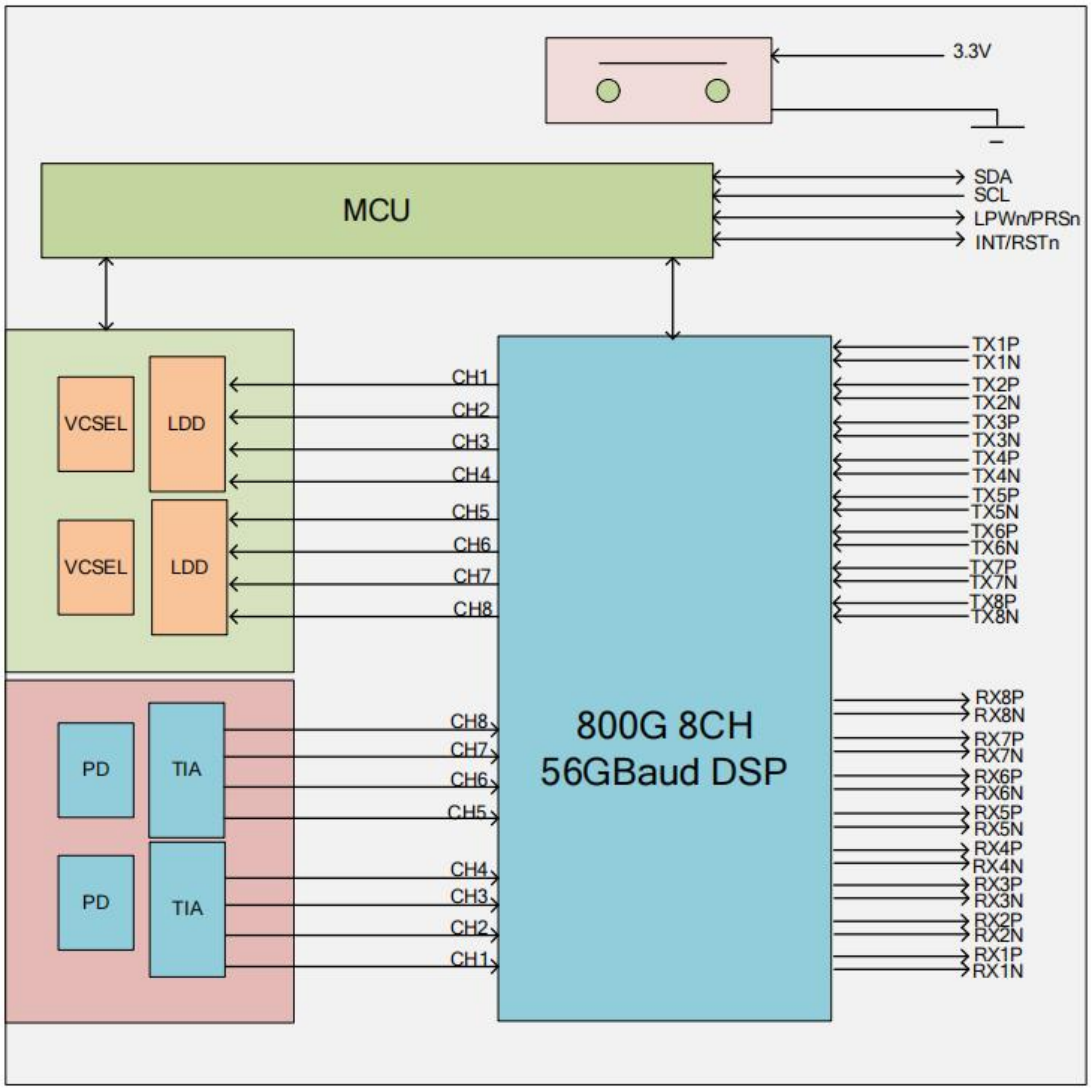
Electrical Interfaces						
Transmitter						
Parameter	**Symbol**	**Min.**	**Typical**	**Max.**	**Unit**	**Note**
Tx_Data Differential Input Voltage	V_{IN}	-	-	900	mV	
Tx_Data Differential Input Impedance	Z_{IN}	-	100	-	Ω	
Receiver						
Parameter	**Symbol**	**Min.**	**Typical**	**Max.**	**Unit**	**Note**
Rx_Data Differential Output Voltage	V_{OUT}	-	-	900	mV	
Rx_Data Differential Output Impedance	Z_{OUT}	-	100	-	Ω	

Optical Characteristics						
Transmitter						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**	**Note**
Signaling rate, each lane	SR	-	53.12	-	Gbd	
Signaling Speed Accuracy	SSA	-100	-	100	ppm	
Modulation format			PAM4			
Average Launch Power ,each lane	P_{OUT}	-4.6	-	4	dBm	Average Optical Output
Outer Optical Modulation Amplitude each lane	OMAouter	-2.6	-	3.5	dBm	
Optical Output with Tx OFF	P_{OFF}	-	-	-30	dBm	
Extinction ratio	ER	2.5	-	-	dB	
Center Wavelength	λ	844	-	868	nm	
RMS Spectral Width	△λ	-	-	0.6	nm	
Transmitter and dispersion eye closure (TDECQ) each lane	TDECQ	-	-	4.4	dB	
Overshoot/undershoot (max)		-	-	29	%	
$RIN_{12}OMA$	$RIN_{12}OMA$	-	-	-132	dB/Hz	
Optical return loss tolerance (Max)	ORLT	-	-	14	dB	
Receiver						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**	**Note**
Signaling rate, each lane	SR	-	53.12	-	Gbd	
Signaling Speed Accuracy	SSA	-100	-	100	ppm	
Modulation format			PAM4			
Average power at receive input, each lane	P_{IN}	-6.4	-	4	dBm	1
Receive power		-	-	3.5	dBm	

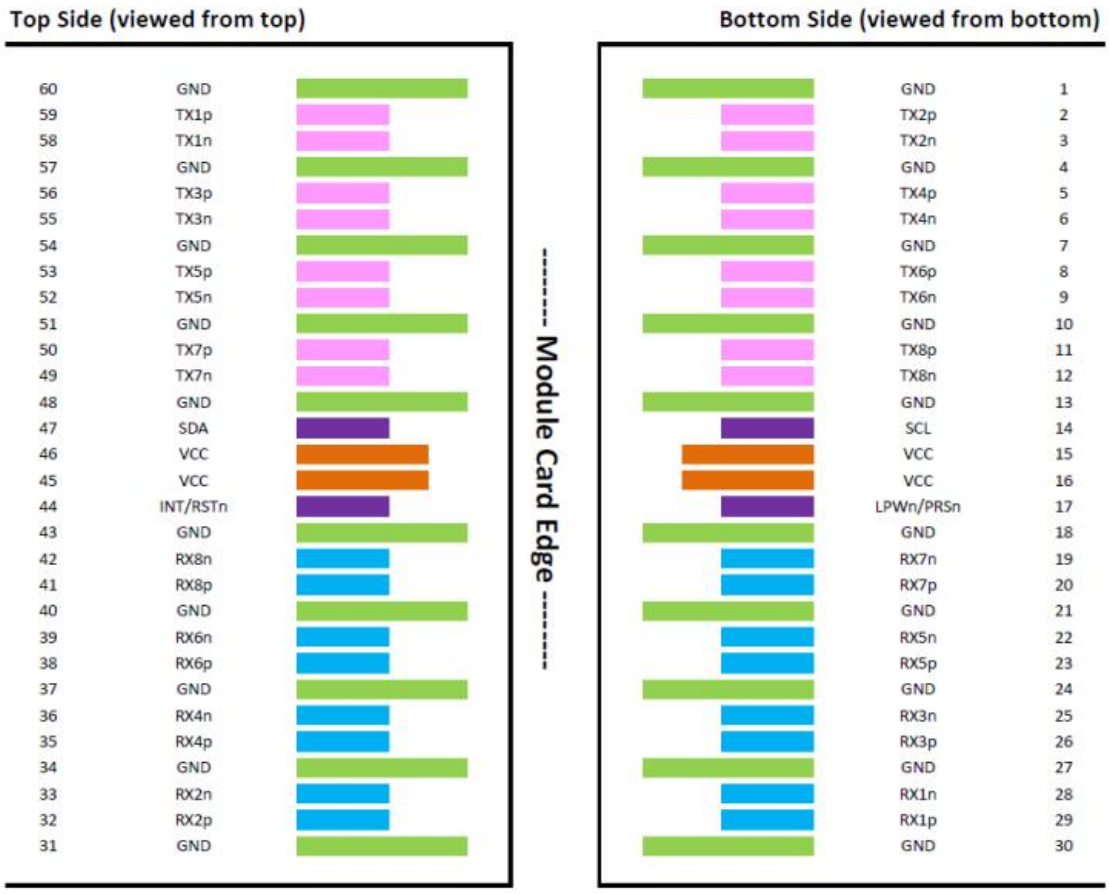
(OMAouter), each lane (max)						
Receiver sensitivity (OMAouter) each lane	Sen	-	-	Max(-4.6, TECQ-6.4)	dBm	2
Center Wavelength	λ	844	-	868	nm	
Rx_LOS of Signal - Assert	P_A	-24.6	-	-	dBm	
Rx_LOS of Signal - Deassert	P_D	-	-	-7	dBm	
Rx_LOS of Signal - Hysteresis	P_H	0.5	-	-	dB	

Notes:
1. Average received power where the BER = 2.4E-4 measured with a PRBS 31Q test pattern@53.12GBaud.
2. Sensitivity where the BER = 2.4E-4 measured with a PRBS 31Q test pattern@53.12GBaud.

Block Diagram



Pin Assignment

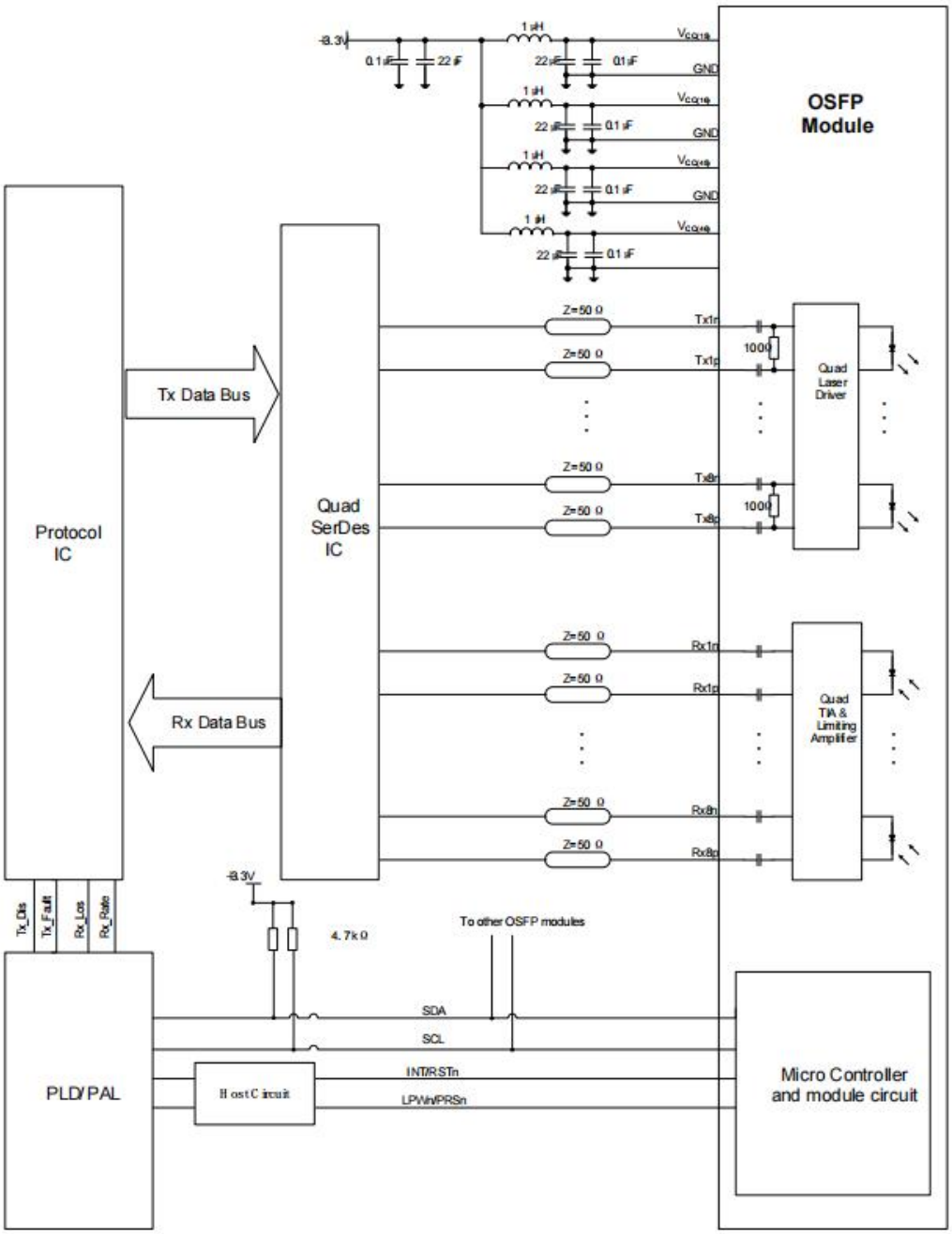


Pin#	Symbol	Description	Logic	Direction	Plug Sequnce	Note
1	GND		Ground		1	
2	TX2p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
3	TX2n	Transmitter Data Inverted	CML-I	Input from Host	3	
4	GND		Ground		1	
5	TX4p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
6	TX4n	Transmitter Data Inverted	CML-I	Input from Host	3	
7	GND		Ground		1	
8	TX6p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
9	TX6n	Transmitter Data Inverted	CML-I	Input from Host	3	
10	GND		Ground		1	
11	TX8p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
12	TX8n	Transmitter Data Inverted	CML-I	Input from Host	3	
13	GND		Ground		1	
14	SCL	2-wire Serial interface clock	LVCMOS-I/ O	Bi-directional	3	1
15	VCC	+3.3V Power		Power from Host	2	
16	VCC	+3.3V Power		Power from Host	2	
17	LPWn/PRSn	Low-Power Mode / Module Present	Multi-Level	Bi-directional	3	2
18	GND		Ground		1	
19	RX7n	Receiver Data Inverted	CML-O	Output to Host	3	
20	RX7p	Receiver Data Non-Inverted	CML-O	Output to Host	3	

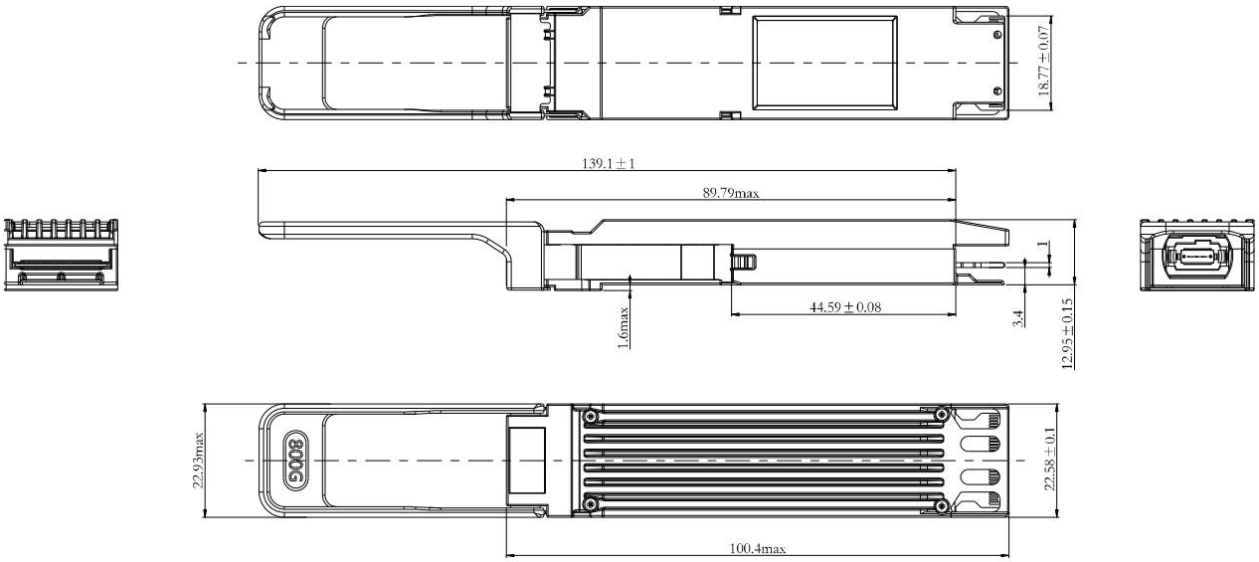
21	GND		Ground		1	
22	RX5n	Receiver Data Inverted	CML-O	Output to Host	3	
23	RX5p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
24	GND		Ground		1	
25	RX3n	Receiver Data Inverted	CML-O	Output to Host	3	
26	RX3p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
27	GND		Ground		1	
28	RX1n	Receiver Data Inverted	CML-O	Output to Host	3	
29	RX1p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
30	GND		Ground		1	
31	GND		Ground		1	
32	RX2p	Receiver Data Inverted	CML-O	Output to Host	3	
33	RX2n	Receiver Data Non-Inverted	CML-O	Output to Host	3	
34	GND		Ground		1	
35	RX4p	Receiver Data Inverted	CML-O	Output to Host	3	
36	RX4n	Receiver Data Non-Inverted	CML-O	Output to Host	3	
37	GND		Ground		1	
38	RX6p	Receiver Data Inverted	CML-O	Output to Host	3	
39	RX6n	Receiver Data Non-Inverted	CML-O	Output to Host	3	
40	GND		Ground		1	
41	RX8p	Receiver Data Inverted	CML-O	Output to Host	3	
42	RX8n	Receiver Data Non-Inverted	CML-O	Output to Host	3	
43	GND		Ground		1	
44	INT/RSTn	Module Interrupt / Module Reset	Multi-Level	Bi-directional	3	3
45	VCC	+3.3V Power		Power from Host	2	
46	VCC	+3.3V Power		Power from Host	2	
47	SDA	2-wire Serial interface data	VCMOS-I/O	Bi-directional	3	1
48	GND		Ground		1	
49	TX7n	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
50	TX7p	Transmitter Data Inverted	CML-I	Input from Host	3	
51	GND		Ground		1	
52	TX5n	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
53	TX5p	Transmitter Data Inverted	CML-I	Input from Host	3	
54	GND		Ground		1	
55	TX3n	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
56	TX3p	Transmitter Data Inverted	CML-I	Input from Host	3	
57	GND		Ground		1	
58	TX1n	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
59	TX1p	Transmitter Data Inverted	CML-I	Input from Host	3	
60	GND		Ground		1	

Notes:
1. Open-Drain with Pull-up resistor on Host
2. LPWn/PRSn is a dual function signal that allows the host to signal Low Power mode and the module to indicate Module Present.
3. INT/RSTn is a dual function signal that allows the module to raise an interrupt to the host and also allows the host to reset the module.

Recommended Interface Circuit



Outline Dimensions



Notes:
1. Tolerance：±0.1 mm.
2. Others according with QSFP112 MSA or customer SPEC.
3. Light port according with fiber connector SPEC

Optical interface arrangement

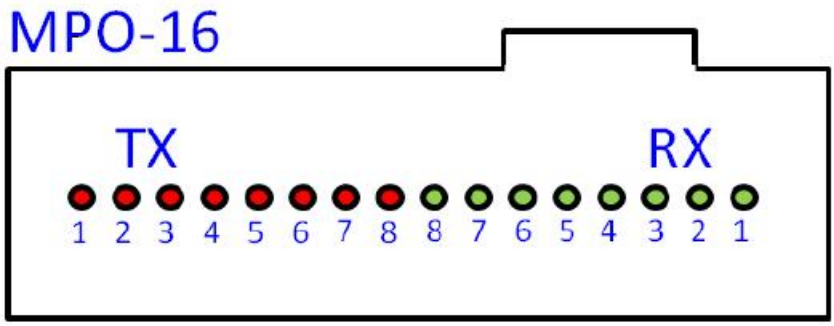


Figure 4 Optical interface arrangement

Order Information

Part Number	Description
S-OS800G31M1601-CD	800G OSFP SR8 Transceiver DDM 0~70℃ MPO