400Gbps QSFP-DD SR4 100m OM3 Optical Transceiver

S-Q64A85M01-CD-4

Features

- QSFP-DD MSA compliant
- 4 parallel lanes
- Optical Interface: IEEE 802.3db compliant
- Electrical Interface: IEEE 802.3 2022400GAUI-8
- Maximum link length of 70m on OM3 or 100m on OM4
- CMIS Compliance
- Operating case temperature: 0 to 70oC
- Support 425Gb/s aggregate bit rate
- Maximum power consumption 8W
- MPO-12 connector

Applications

- Ethernet
- Telecom

Description

400Gb/s QSFP56-DD SR4 optical module.This product is a 400Gb/s Quad Small Form Factor Pluggable-double density (QSFP56-DD) optical module designed for 100m optical communication applications. The module converts 8 channels of 50Gb/s (PAM4) electrical input data to 4 channels of optical signals,and multiplexes them into a single channel for 400Gb/s optical transmission. Reversely, on the receiver side, the module optically de-multiplexes a 400Gb/s optical input into 4 channels of optical signals, and converts them to 8 channels of 50Gb/s (PAM4) electrical output data.

An optical fiber cable with an MPO-12 connector can be plugged into the QSFP56-DD SR4 module receptacle. Proper alignment is ensured by the guide pins inside the receptacle. The cable usually cannot be twisted for proper channel to channel alignment. Electrical connection is achieved through a QSFP56-DD MSA-compliant edge type connector.

This product is designed with form factor, optical/electrical connection and digital diagnostic interface according to the QSFP56-DD MSA Type2. It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference.

Functional Description

The transceiver complies with common management interface specification (CMIS). The supported key features listed below allow host software to read and control the transceiver status through I2C.

- Adaptive Tx input equalization
- Programmable Rx output amplitude
- Programmable Rx output pre-cursor
- Programmable Rx output post-cursor

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- Supply voltage monitoring (DDM_Voltage)
- Transceiver case temperature monitoring (DDM_Temperature)
- Tx transmit optical power monitoring for each lane (DDM_TxPower)
- Tx bias current monitoring for each lane (DDM_TxBias)
- Rx receive optical power monitoring for each lane (DDM_RxPower)
- Warning and alarm indication for each DDM function
- Tx & Rx LOL and LOS indication
- Tx fault indication
- Host and line side loopback capabilities
- Host and line side PRBS generator and checker capabilities
- CDB firmware upgrade capability
- Versatile diagnostics monitoring (VDM) capability (optional, additional power consumption increase)
- Other functions defined in CMIS

Transceiver Block Diagram

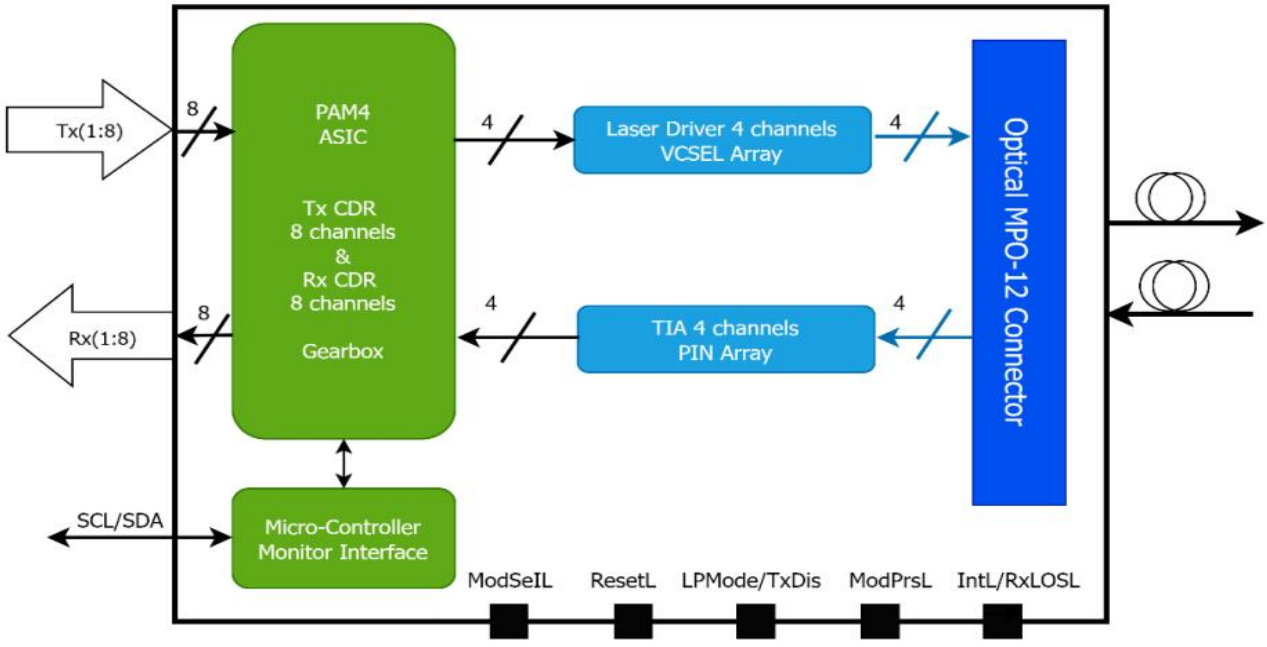

Figure 1. Transceiver Block Diagram

Optical interface and Pin Assignment

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The electrical interface of QSFP-DD module consist of a 76 contacts edge connector as illustrated by the diagram in Figure 2, which defined in Clause 4.1 of QSFP-DD MSA Specification.

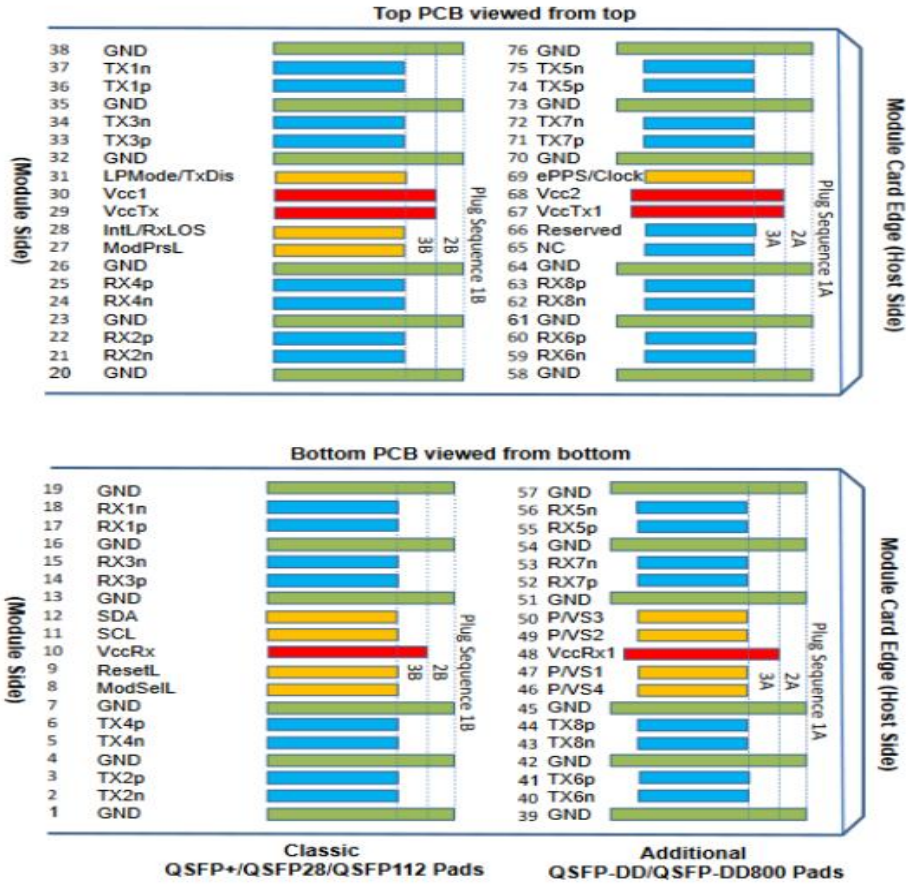

Figure 2. MSA Compliant Connector

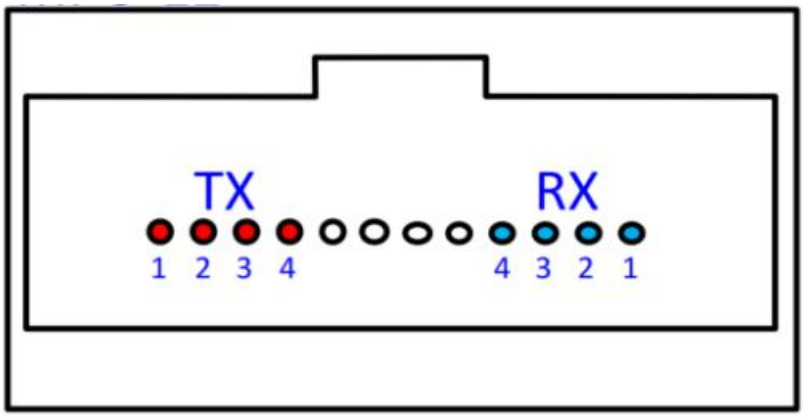

Figure 3. MPO-12 Optical Connector Interface

Pin Definition

Pin #	Logic	Symbol	Description	Plug Sequence

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1		GND	Ground	1B
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B
4		GND	Ground	1B
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B
6	CML-I	Tx4P	Transmitter Non-Inverted Data Input	3B
7		GND	Ground	1B
8	LVTTL-I	ModSelL	Module Select	3B
9	LVTTL-I	ResetL	Module Reset	3B
10		VccRx	+3.3V Power Supply Receiver	2B
11	LVCMOS-I/O	SCL	TWI serial interface clock	3B
12	LVCMOS-I/O	SDA	TWI serial interface data	3B
13		GND	Ground	1B
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B
15	CML-O	Rx3n	Receiver Inverted Data Output	3B
16		GND	Ground	1B
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B
18	CML-O	Rx1n	Receiver Inverted Data Output	3B
19		GND	Ground	1B
20		GND	Ground	1B
21	CML-O	Rx2n	Receiver Inverted Data Output	3B
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B
23		GND	Ground	1B
24	CML-O	Rx4n	Receiver Inverted Data Output	3B
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B
26		GND	Ground	1B
27	LVTTL-O	ModPrsL	Module Present	3B
28	LVTTL-O	IntL/RxLOS	Interrupt/optional RxLOS	3B
29		VccTx	+3.3V Power supply transmitter	2B
30		Vcc1	+3.3V Power supply	2B
31	LVTTL-I	LPMode/TxDis	Low Power mode/optional TX Disable	3B
32		GND	Ground	1B
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B
35		GND	Ground	1B
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B
38		GND	Ground	1B

39		GND	Ground	1A
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A
42		GND	Ground	1A
43	CML-I	Tx6n	Transmitter Inverted Data Input	3A
44	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A
45		GND	Ground	1A
46	LVCMOS/CML-I	P/VS4	Programmable/Module Vendor Specific 4	3A
47	LVCMOS/CML-I	P/VS1	Programmable/Module Vendor Specific 1	3A
48		VccRx1	3.3V Power Supply	2A
49	LVCMOS/CML-O	P/VS2	Programmable/Module Vendor Specific 2	3A
50	LVCMOS/CML-O	P/VS3	Programmable/Module Vendor Specific 3	3A
51		GND	Ground	1A
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A
53	CML-O	Rx7n	Receiver Inverted Data Output	3A
54		GND	Ground	1A
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A
56	CML-O	Rx5n	Receiver Inverted Data Output	3A
57		GND	Ground	1A
58		GND	Ground	1A
59	CML-O	Rx5n	Receiver Inverted Data Output	3A
60	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A
61		GND	Ground	1A
62	CML-O	Rx8n	Receiver Inverted Data Output	3A
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A
64		GND	Ground	1A
65		NC	No Connect	3A
66		Reserved	For future use	3A
67		VccTx1	3.3V Power Supply	2A
68		Vcc2	3.3V Power Supply	2A
69	LVCMOS-I	ePPS/Clock	1PPS PTP clock or reference clock input	3A
70		GND	Ground	1A
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A
73		GND	Ground	1A
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A
76		GND	Ground	1A

Recommended Power Supply Filter

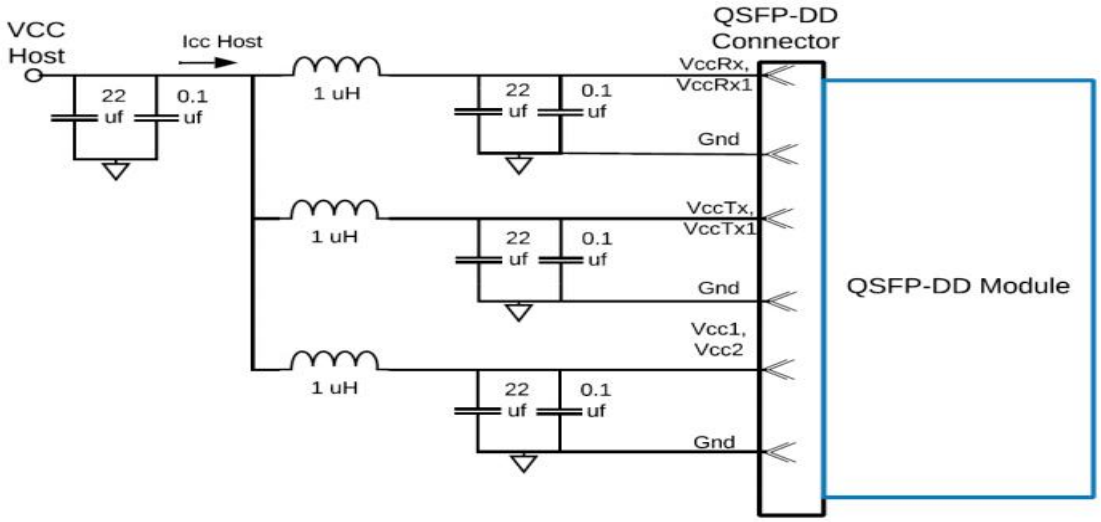

Figure 4.Recommended Power Supply Filter

Absolute Maximum Ratings

It hasto be noted that the operation in excess of any individual absolute maximum ratings might cause permanent damage to this module.

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	Vcc	-0.5		3.6	V
Storage Temperature	Ts	-40		85	°C
Operating Case Temperature	To	0		70	°C
Relative Humidity (non-condensation)	RH	0		85	%

Recommended Operating Conditions and Power Supply Requirements

Parameter	Symbol	Min	Typical	Max	Units	Notes
Operating Case Temperature	TOP	0		70	degC	
Power Supply Voltage	VCC	3.135	3.3	3.465	V	
Data Rate, each Lane			53.125		GBd	PAM4
Data Rate Accuracy		-100		100	ppm	
Link Distance with OM3	D1	2		70	m	1
Link Distance with OM4	D2	2		100	m	2

Notes

1. FEC provided by host system.
2. FEC required on host system to support maximum distance.

Electrical Characteristics

The following electrical characteristics are defined over the Recommended Operating Environment unless otherwise specified.

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Parameter	Test Point	Min	Typical	Max	Units	Notes
Power Consumption				8	W	
Supply Current	Icc			2.55	A	
Transmitter (each Lane)						
Signaling Rate, each Lane	TP1	26.5625 ± 100 ppm			GBd	
Differential pk-pk Input Voltage Tolerance Mismatch	TP1a	900			mVpp	1
Differential Termination	TP1			10	%	
Differential Input Return Loss	TP1	IEEE 802.3-2015 Equation (83E-5)			dB	
Differential to Common Mode Input Return Loss	TP1	IEEE 802.3-2015 Equation (83E-6)			dB	
Module Stressed Input Tes	TP1a	See IEEE 802.3bs 120E.3.4.1				2
Single-ended Voltage Tolerance Range (Min)	TP1a	-0.4 to 3.3			V	
Dc Common Mode Input Voltage	TP1	-350		2850	mV	3
Tolerance Range (Min)						
Signaling Rate, each Lane	TP4	26.5625 ± 100 ppm			GBd	
Differential Peak-to-Peak Output Voltage	TP4			900	mVpp	
AC Common Mode Output Voltage, RMS	TP4			17.5	mV	
Differential Termination Mismatch	TP4			10	%	
Differential Output Return Loss	TP4	IEEE 802.3-2015 Equation (83E-2)			db	
Common to Differential Mode Conversion Return Loss	TP4	IEEE 802.3-2015 Equation (83E-3)			db	
Transition Time, 20% to 80%	TP4	9.5			ps	
Near-end Eye Symmetry Mask Width (ESMW)	TP4		0.265		UI	
Near-end Eye Height, Differential	TP4	70			mV	
Far-end Eye Symmetry Mask Width (ESMW)	TP4		0.2		UI	
Far-end Eye Height, Differential	TP4	30			mV	
Far-end Pre-cursor ISI Ratio	TP4	-4.5		2.5	%	
Common Mode Output Voltage (Vcm)	TP4	-350		2850	mV	3
Notes:						
1. With the exception to IEEE 802.3bs 120E.3.1.2 that the pattern is PRBS31Q or scrambled idle. 2. Meets BER specified in IEEE 802.3bs 120E.1.1. 3. DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.						

Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Units	Notes
Transmitter						

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Center Wavelength	λC	840	850	860	nm	
Data Rate, each Lane		53.125 ± 100 ppm			GBd	
Modulation Format		PAM4				
RMS Spectral Width	Δλrms			0.6	nm	1
Average Launch Power, each Lane	P_{AVG}	-4.6		4	dBm	
Outer Optical Modulation Amplitude (OMAouter), each Lane	P_{OMA}	-2.6(For max (TECQ, TDECQ) ≤1.8 dB)-4.4 + max(TECQ,TDECQ) (For 1.8 < max (TECQ, TDECQ) ≤ 4.4 dB)		3.5	dBm	
Transmitter and Dispersion Eye Clouser for PAM4,each Lane	TDECQ			4.4	dB	
Transmitter Eye Clouser for PAM4,each Lane	TECQ			4.4	dB	
Overshoot/undershoot				29	%	
Transmitter power excursion, each Lane				2.3	dBm	
Extinction Ratio	ER	2.5			dB	
Transition Time	T_t			17	ps	
$RIN_{14}OMA$	RIN			-132	db/Hz	
Optical Return Loss Tolerance	TOL			14	dB	
Average Launch Power of OFF Transmitter, each Lane	P_{off}			-30	dBm	
Encircled Flux		≥ 86% at 19 μm ≤ 30% at 4.5 μm				2
Receiver						
Center Wavelength	λC	840	850	860	nm	
Data Rate, each Lane		53.125 ± 100 ppm			GBd	
Modulation Format		PAM4				
Damage Threshold, each Lane	THd	5			dBm	3
Average Receive Power, each Lane		-6.4		4	dBm	4
Receive Power (OMA_{outer}), each Lane				3.5	dBm	
Receiver Sensitivity (OMA_{outer}), each Lane	SEN			-4.6(For TECQ ≤ 1.8 dB)–6.4 +TECQ（For 1.8 ＜TECQ ≤ 4.4 dB)	dBm	5
Stressed Receiver Sensitivity(OMAouter), each Lane	SRS			-2	dBm	6
Receiver Reflectance	R_R			-15	dB	
LOS Assert	LOSA	-15			dBm	
LOS De-assert	LOSD			-9	dBm	
LOS Hysteresis	LOSH	0.5			dB	
Stressed Conditions for Stress Receiver Sensitivity (Note 7)						

Stressed Eye Closure for PAM4 (SECQ), Lane under Test			4.4		dB	
OMA_{outer} of each Aggressor Lane			3.5		dBm	

Notes:

1. RMS spectral width is the standard deviation of the spectrum.
2. If measured into type A1a.2 or type A1a.3, or A1a.4, 50 µm fiber, in accordance with IEC 61280-1-4.
3. The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.
4. Average receive power, each lane (min) is informative and not the principal indicator of signal strength.A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
5. Receiver sensitivity (OMAouter) is informative and is defined for a transmitter with a value of TECQ up to 4.4 dB. Receiver sensitivity should meet Equation (1), which is illustrated in Figure 5.

   RS= max(−4.6,TECQ-6.4) dbm

   Where:
   RS is the receiver sensitivity, and
   TECQ is the TECQ of the transmitter used to measure the receiver sensitivity.
6. Measured with conformance test signal at TP3 for the BER equal to $2.4x10^{-4}$.
7. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

Digital Diagnostic Functions

The following digital diagnostic characteristics are defined over the normal operating conditions unless otherwise specified.

Parameter	Symbol	Min	Max	Units	Notes
Temperature monitor absolute error	DMI_Temp	-3	3	degC	Over operating temperature range
Supply voltage monitor absolute error	DMI _VCC	-0.1	0.1	V	Over full operating range
Channel RX power monitor absolute error	DMI_RX_Ch	-2	2	dB	1
Channel Bias current monitor	DMI_Ibias_Ch	-10%	10%	mA	
Channel TX power monitor absolute error	DMI_TX_Ch	-2	2	dB	1

Notes:

1. Due to measurement accuracy of different single mode fibers, there could be an additional +/-1 dB fluctuation, or a +/- 3 dB total accuracy.

Mechanical Dimensions

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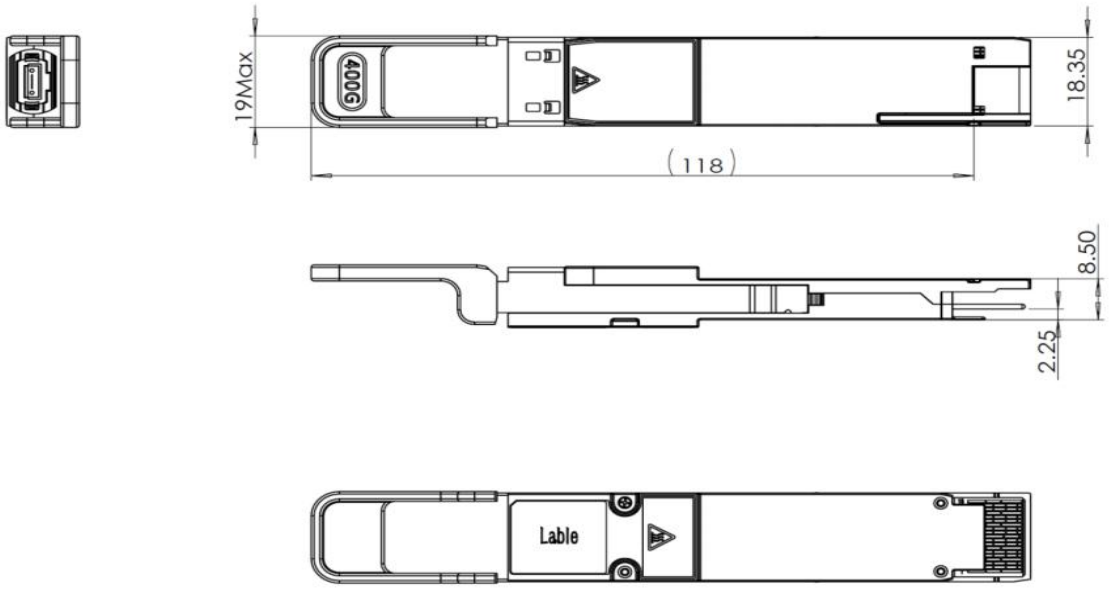

Figure 5. Mechanical Outline

ESD

This transceiver is specified as ESD threshold 1kV for high speed data pins and 2kV for all other electrical input pins, tested per MIL-STD-883, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

Laser Safety

This is a Class 1 Laser Product according to EN 60825-1:2014.

This product complies with 21 CFR 1040.10 and 1040.11 except for conformance with IEC 60825-1 Ed.3., as described in Laser Notice No. 56, dated May 8, 2019.

Caution: Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

Ordering information

Part Number	Product Description
S-Q64A85M01-CD-4	QSFP56-DD 400G 850nm SR4 100M MPO-12, 0ºC~+70ºC, With DDM